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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,954	07/24/2003	Gerald G. Fagerness	ROC920030054US1	1614

30206 7590 06/10/2008

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2619	

MAIL DATE	DELIVERY MODE
06/10/2008	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/625,954
Filing Date: July 24, 2003
Appellant(s): FAGERNESS ET AL.

Steven M. Santisi (Reg. No. 40,157)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/28/2008 appealing from the Office action mailed 11/28/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,414,701	SHTAYER et al	5-1995
6,356,552	FOGLAR	3-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **16-19** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,414,701 to Shtayer et al.

Regarding claim **16**, Shtayer discloses a method for address mapping in a network processor, the method comprising: determining a port number of a port that receives a data cell (the PHY/LINK Id 14 of Figures 1, 3, and 5); determining a virtual path identifier and a virtual channel identifier for the data cell (see lines 64-68 of column 5 and lines 30-34 of column 6); creating a first index based on at least one of the port number, the virtual path identifier and the virtual channel identifier (the PHY/LINK Id is used to index the link table in Figures 3 and 5);

accessing one of a plurality of entries stored in a first on-chip memory using the first index (the PHY/LINK Id is used to index the link table in Figures 3 and 5); creating a second index based on the accessed entry of the first on-chip memory (see Figure 3 – the VP Index is created using the VP_MASK of the link table entry); and accessing an entry of a second memory based on the second index (see Figure 3 – the Link VP Table is accessed using this second index (VP Index)).

Similarly, regarding claim **18**, Shtayer discloses a system adapted to perform address mapping in a network processor comprising: a first on-chip memory having a plurality of entries (the link table of Figure 3); and a logic circuit adapted to: create a first index based on at least one of a number of a port that receives a data cell, a virtual path identifier for the data ceil and a virtual channel identifier for the data cell (the PHY/LINK Id is used to index the link table in Figures 3 and 5); access one of the plurality of entries stored in the first on-chip memory using the first index (see lines 33-52 of column 5); and create a second index based on the accessed entry of the first on-chip memory (see Figure 3 – the VP Index is created using the VP_MASK of the link table entry).

Regarding claims **17 and 19**, Shtayer discloses the limitation that each entry stored in the first on-chip memory contains a base address field (the VP_POINTER field) and one or more of a number of port number bits field, a number of virtual path identifier bits field and a number of virtual channel identifier bits field (the VP_MASK field, as indicated in figure 4, indicates the number of VPI bits to be used).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims **1-3 and 5-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,414,701 to Shtayer, et al in view of U.S. Patent 6,356,552 to Foglar.

Regarding claims **1 and 11**, Shtayer discloses a method and system for determining a control block index for a data cell received by a network processor coupled to an ATM network comprising (see figures 3 and 5): receiving a data cell at a port, the data cell having a virtual path identifier and a virtual channel identifier (see figure 1 and lines 36-39 of column 4); determining a port number for the port (the PHY/LINK Id; see lines 36-40 of column 5, for example); employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create a first address (the PHY/LINK Id is used as the first address; see lines 36-40 of column 5); employing the first address to access a first memory and to obtain a first entry from the first memory (the entry in the Link Table of Figure 3), the first entry specifying: a first base memory address (the VP POINTER element of this entry); a number of bits of the virtual path identifier to use in the control block index (the VP_MASK field, as indicated in figure 4,

indicates the number of VPI bits to be used). These sections of Shtayer also disclose the analogous limitations of claim 11.

However, Shtayer does not disclose expressly the limitation that the first entry specifies a number of bits of the port number to use in the control block index and a number of bits of the virtual channel identifier to use in the control block index; or the limitation of employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create a control block index for the data cell.

However, Foglar does disclose these limitations. Specifically, Foglar discloses a number of bits of the port number to use in the control block index (P bits; see figure 1); a number of bits of the virtual path identifier to use in the control block index (14-M bits; see figure 1); and a number of bits of the virtual channel identifier to use in the control block index (M-P bits; see figure 1). Foglar also discloses the limitation of employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create the control block index for the data cell (this is disclosed in the generation of the 14-bit LCI index throughout – see Figure 1, for example). Shtayer and Foglar are analogous art because they are from the same field of endeavor of ATM switching. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Shtayer to compress the multistage method of Shtayer (see Figure 3) to a single stage LCI generation method like that of Foglar. The motivation for doing so would have been to reduce the hardware complexity (and thus cost) required by the multistage scheme like Shtayer as suggested by Foglar in the background section – see lines 23-30 of column 3. Therefore, it

would have been obvious to combine Foglar with Shtayer for the benefit of reducing hardware complexity (and thus cost) to obtain the invention as specified in claims 1 and 11.

Regarding claim **2**, the above combination clearly discloses the limitation that employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create the first address comprises employing bits of at least one of the virtual path identifier and the port number to create the first address as shown in Figure 1 of Foglar. Clearly, the VPI and port number are used in the creation of the LCI.

Regarding claims **3 and 12**, Shtayer discloses the limitation that the first memory is an on-chip memory of the network processor throughout – see figures 2 and 3, for example, which describe the link table as internal.

Regarding claims **5 and 13**, Shtayer does not disclose expressly the limitations of these claims. However, Foglar discloses the limitations that employing the first base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the first entry to create the control block index for the data cell comprises: selecting the number of bits of the port number specified by the first entry (see figure 1 – the P pits of port number PN are selected); selecting the number of bits of the virtual path identifier specified by the first entry (see figure 1 – the 14-M bits of the VPI are selected); selecting the number of bits of the virtual channel identifier specified by the first entry (see figure 1 – the M-P bits of the VCI are selected); catenating any selected bits (see lines 1-5 of column 6); and adding the catenated selected bits to the first base memory address (this is well known and taught in Shtayer (lines 22-25 of column 5); it is also clearly the intent of Foglar as the 14 bit LCI is intended to be able to identify 16 K connections (see lines 32-35 of column 5) and this is not possible unless the LCI is

an offset from a base address (unless all 16 K addresses are stored at physical memory address zero which is impractical)). Shtayer and Foglar are analogous art because they are from the same field of endeavor of ATM switching. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Shtayer to compress the multistage method of Shtayer (see Figure 3) to a single stage LCI generation method like that of Foglar. The motivation for doing so would have been to reduce the hardware complexity (and thus cost) required by the multistage scheme like Shtayer as suggested by Foglar in the background section – see lines 23-30 of column 3. Therefore, it would have been obvious to combine Foglar with Shtayer for the benefit of reducing hardware complexity (and thus cost) to obtain the invention as specified in claims 5 and 13.

Regarding claims **6 and 14**, the above combination of Shtayer and Foglar does not disclose expressly the limitations of shifting the control block index; and adding the shifted control block index to a main system memory base offset so as to generate a control block memory address. However, this would have been obvious to one of ordinary skill in the art and necessary for the above combination. In order for the above mentioned LCI (14 bits) to access 16 K entries where the entries are larger than one byte in size, the offset will need to be shifted by one or more bits prior to being added to the base address in order to properly identify the location in memory. At the time of the invention, it would have been obvious to one of ordinary skill in the art to explicitly perform this shifting of the index. The motivation for doing so would have been to allow the combination of Shtayer and Foglar to properly locate a memory entry of larger than one byte using the LCI index. Therefore, it would have been obvious to modify the

combination of Shtayer and Foglar for the benefit of storing more information than a single byte per connection to obtain the invention as specified in claims 6 and 14.

Regarding claim **7**, Shtayer discloses the limitation of employing the control block memory address to obtain a control block from a main system memory in Figure 2 which shows that the link table is internal memory (to the chip); the other tables are thus clearly stored in external or main memory and thus the control block address is used to obtain the control block from main memory.

Regarding claim **8**, the combination of Shtayer and Foglar as described above discloses all limitations of parent claim 5. This combination does not explicitly disclose the limitation of this claim. However, Foglar discloses the limitation of verifying that non-selected port number, virtual path identifier and virtual channel identifier bits are zeroed in the passage from line 59 of column 8 through line 4 of column 9. Shtayer and Foglar are analogous art because they are from the same field of endeavor of ATM switching. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the previous combination of Shtayer and Foglar to verify that the non-selected bits are zeroed. The motivation for doing so would have been to detect and handle errors as suggested by Foglar in the passage from line 59 of column 8 through line 4 of column 9. Therefore, it would have been obvious to combine Foglar with Shtayer for the benefit of detecting and handling errors to obtain the invention as specified in claim 8.

Regarding claim **9**, Shtayer discloses the limitation of pre-selecting which bits are used to form the first address in lines 36-39 of column 5 which indicates that all bits are used to form the first address and that this is pre-determined.

Regarding claim **10**, Shtayer discloses the limitation of selecting each entry for the first memory in lines 33-61 of column 5 which describes how each field of each entry is selected.

Regarding claim **15**, Shtayer discloses the limitations of determine each entry within the first memory (see lines 33-61 of column 5 which describes how each field of each entry is selected); and determine which bits of a port number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell are employed to generate an address for the first memory (see lines 36-39 of column 5 which indicates that all bits are used to form the first address and that this is pre-determined).

Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,414,701 to Shtayer, et al in view of U.S. Patent 6,356,552 to Foglar and in further view of U.S. Patent 6,272,504 to Baentsch et al.

As disclosed above, the combination of Shtayer and Foglar discloses all limitations of parent claim 3 and thus the limitation of claim 4 that the first memory is on-chip. However, the combination of Shtayer and Foglar does not disclose expressly that the first memory comprises a random access memory. However, Baentsch discloses the advantage of random access memory in lines 8-10 of column 2. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Shtayer and Foglar to explicitly use random access memory (RAM) for the link table. The motivation for doing so would have been to provide faster memory access as suggested by Baentsch in lines 9-10 of column 2. Therefore, it would have been obvious to combine Baentsch with Shtayer and Foglar for the benefit of faster memory access to obtain the invention as specified in claim 4.

(10) Response to Argument

In section A on pages 11-12, Appellant addresses the rejection of independent claims 1 and 11 under 35 U.S.C. 103(a) over U.S. Patent 5,414,701 to Shtayer, et al in view of U.S. Patent 6,356,552 to Foglar.

In the first few paragraphs of this section, Appellant recites a subset of the limitations of claims 1 and 11 and asserts that the combination of Shtayer and Foglar fails to disclose at least these limitations.

The next few paragraphs indicate that Appellant disagrees with Examiner's assertion that the Foglar reference discloses the limitation that a first entry specifies a number of bits of the port number to use in the control block index. Specifically, Appellant has issue with use of the variable "P" of the Foglar reference to disclose this limitation. Appellant argues that P is defined to mean something else. On page 12, Appellant indicates that Foglar discloses generating a logical channel identifier from 3 parameters which include a physical port number (PN). In the following paragraph, Appellant cites portions of Foglar which appear to indicate that P is defined as "the number of lines or termination units".

Examiner respectfully disagrees with Appellant's misleading characterization of Foglar. Appellant has deleted portions of the citation which are material to his argument. In particular, Foglar indicates specifically in lines 27-29 of column 7 that "In the example in question, ***2^P is equal to the number of lines or termination units***" (emphasis added). This is presumably the passage that Appellant cited when asserting that P was equal to the number of lines or termination units. This passage actually supports Examiners position that P is the number of bits

in the port number. For example, if the value of P is 3, the port number parameter is 3 bits long (***P bits long***) and will support $8=2^P$ ports (or lines or termination units). Further, Figures 1 and 2 which were cited in the Final rejection clearly support Examiner's position as they both show the logical channel identifier as containing a field which is "P bits" long. This clearly indicates that ***P is a number of bits*** rather than a number of ports or lines or termination units as suggested by Appellant.

In the next paragraph, Appellant argues that Examiner has indicated in a previous office action that P was equal to a number of ports. However, Applicant has incorrectly copied the citation from the office action. The citation in fact supports the Examiner's position as it states "The value of P is clearly the number of ***port bits*** used in the creation of the LCI" (emphasis added).

Appellant summarizes by stating that the aforementioned limitation regarding a number of bits in a port number id different than P in Foglar. Examiner respectfully disagrees. As indicated above, Appellants arguments are based on misleading and incorrect information and thus are not valid. Examiner's rejection is correct and the limitation in question is disclosed by Foglar.

In section B on pages 13-14, Appellant addresses the rejection of independent claims 16 and 18 under 35 U.S.C. 102(b) over U.S. Patent 5,414,701 to Shtayer, et al.

In the first four paragraphs of this section, Appellant recites a subset of the limitations of these claims and indicates that the main limitation at issue is that of the entries being stored in "on-chip memory". Applicant asserts that the interpretation of the "Internal" notation used in the

Final rejection is contrary to how one of ordinary skill in the art would have interpreted the notation. Examiner respectfully disagrees. First, Shtayer shows several tables in Figures 2, 3, and 5. Only the link table has the notation "Internal". Clearly, Shtayer is differentiating a property of this table from the similar properties of the other tables. Shtayer does not go into a lot of detail about this "Internal" property of the link table as it is not the novelty of his invention. However, it is evident to one of ordinary skill in the art that this is taken to mean the location of the table (i.e. "Internal" to the processing device). Shtayer emphasizes in numerous places that the Link VP and VC Tables are stored ***in memory*** (see lines 6-10 of column 2, for example). This language is used in the art to indicate a separate memory device (different than the small amount of memory typically available internal to the processing device itself (i.e. on-chip memory)). Applicant uses this passage (and the numerous other similar passages) to distinguish the location of these tables from that of the link table (which is "Internal" to the processing device (and thus on-chip) as indicated in the figures themselves.)

In the fifth paragraph on page 13, Appellant argues that the notation "Internal" indicates that the entries in the table are stored "in the link table itself". However, this does not make any sense. The entries of any table are stored in the table itself; there would be absolutely no need for Shtayer to indicate that the entries of the table are stored in the table. Further, as indicated above, Shtayer only uses the "Internal" notation on one of the many tables in Figure 2, 3, and 5. Appellant is clearly suggesting that the other tables must therefore store their entries somewhere other than in the table. If the "Internal" notation on the link table indicates that the entries in this table are stored "in the link table itself" (as proposed by Appellant), the consistent absence of this notation from all other tables in the Figures can only mean that the entries in all the other

tables are somehow stored ***outside*** of the tables. It is not clear how this can be the case or how one of ordinary skill in the art would interpret the "Internal" notation to mean that the entries are stored in the table.

Appellant also indicates that Shtayer does not connect these notations with a location of the table. However, as stated above, Examiner believes Shtayer does not spend a lot of energy describing the meaning of Internal as it is not the novelty of the invention. However, Shtayer clearly contrasts the location of the link table (labeled "Internal" in Figures 2, 3, and 5) with the location of the other tables. The location of the other tables is stated throughout as "in memory"; see lines 6-10 of column 2, for example. This language is used in the art to indicate a separate memory device (different than the small amount of memory typically available internal to the processing device itself (i.e. on-chip memory)). Applicant uses this passage (and the numerous other similar passages) to distinguish the location of these tables from that of the link table (which is "Internal" to the processing device as indicated in the figures themselves.)

In the sixth paragraph on page 13 (which continues on page 14), Appellant continues this argument. For reasons stated above, Examiner respectfully disagrees. As indicated above, this logic would imply that the other tables in these figures have their entries stored somewhere other than in the table.

In the next paragraph, Appellant summarizes the arguments of the previous page. Examiner respectfully disagrees for reasons stated above.

In the next 2 paragraphs, Appellant makes similar arguments to rebut Examiner's arguments contained in the Advisory Action. Examiner has expressed his position above and thus clearly disagrees with Appellant.

Appellant proposes reasons why the "Internal" notation is consistently missing from the other tables as being due to the nature of the data being stored in these tables. However, these tables contain information in the entries stored in the table. The fact remains that if the "Internal" notation on the link table indicates that the entries in this table are stored "in the link table itself" (as proposed by Appellant), the consistent absence of this notation from all other tables can only mean that the entries in all the other tables are somehow stored ***outside*** of the tables. This is clearly not logical and is not an interpretation one of ordinary skill in the art would make upon reviewing Shtayer.

Examiner believes the interpretation provided in the Final rejection and further explained above is correct and that the Shtayer reference anticipates the invention as stated in claims 16 and 18.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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